USING REDUNDANT ROUTING TO REDUCE SUSCEPTIBILITY TO SINGLE EVENT UPSETS IN PLD DESIGNS

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ABSTRACT

Methods of implementing designs in programmable logic devices (PLDs) to reduce susceptibility to single-event upsets (SEUs) by taking advantage of the fact that most PLD designs leave many routing resources unused. The unused routing resources can be used to provide duplicate routing paths between source and destination of signals in the design. The duplicate paths are selected such that an SEU in a routing multiplexer included in each path simply switches the signal between the two paths. Thus, if one path is disabled due to an SEU, the other path can still provide the necessary connection, and the functionality of the design is unaffected. The methods can be applied, for example, to routing software for field programmable gate arrays (FPGAs) having programmable routing multiplexers controlled by static RAM-based configuration memory cells.